EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark A. Dalla Valle, Reg. No. 34,147 on November 7, 2008.

2. The application has been amended as follows:

In the claim: Please amend claims 23, 25, 27 and 35 as follow

23. A method for suspending operation of a pipelined data processor including a pipeline subcircuit to reduce power consumption, comprising:

receiving an enabled first clock signal;

receiving one or more data processing instructions with a first portion of said pipeline subcircuit;

executing said one or more data processing instructions in response to said enabled first clock signal with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion; and

receiving an operation suspension instruction with said first pipeline subcircuit portion and in response thereto

preventing advancement of an instruction unrelated to said one or more data processing instructions into said second pipeline subcircuit portion, and

asserting one or more control signals from said pipeline subcircuit, followed by

disabling said first clock signal and thereby suspending execution of any instructions by said second pipeline subcircuit portion, including said executing of said one or more data processing instructions.

25. A method for suspending operation of a pipelined data processor including a pipeline subcircuit to reduce power consumption, comprising:

receiving an enabled first clock signal;

receiving one or more data processing instructions with a first portion of said pipeline subcircuit;

executing said one or more data processing instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal;

receiving an operation suspension instruction with said first pipeline subcircuit portion and in response thereto

asserting one or more control signals from said pipeline subcircuit, followed by

disabling said first clock signal;

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing of said one or more data processing instructions; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

27. A method for suspending operation of a pipelined data processor including a pipeline subcircuit to reduce power consumption, comprising:

receiving an enabled first clock signal;

receiving one or more data processing instructions with a first portion of said pipeline subcircuit;

executing said one or more data processing instructions with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion in response to said enabled first clock signal;

receiving an operation suspension instruction with said first pipeline subcircuit portion and in response thereto

asserting one or more control signals from said pipeline subcircuit, followed by

disabling said first clock signal;

prior to said asserting one or more control signals, completing executing one or more of said one or more data processing instructions which had been received prior to said receiving said operation suspension instruction;

generating, with said pipeline subcircuit in response to said enabled first clock signal, a plurality of data corresponding to said executing one or more of said one or more data processing instructions; and

retaining, with said pipeline subcircuit, said plurality of data in response to said disabled first clock signal.

35. A method for suspending operation of a pipelined data processor including a pipeline subcircuit to reduce power consumption, comprising:

receiving an enabled first clock signal;

receiving one or more data processing instructions with a first portion of said pipeline subcircuit;

executing said one or more data processing instructions in response to said enabled first clock signal with a second portion of said pipeline subcircuit subsequent to said first pipeline subcircuit portion; and

receiving an operation suspension instruction with said first pipeline subcircuit portion and in response thereto

preventing advancement of an instruction unrelated to said one or more data processing instructions into said second pipeline subcircuit portion, and

asserting one or more control signals from said first pipeline subcircuit portion, followed by

disabling said first clock signal and thereby suspending execution of any instructions by said second pipeline subcircuit portion, including said executing of said one or more data processing instructions.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Du whose telephone number is (571) 272-3673. The examiner can normally be reached on Monday-Friday: 7:30 AM - 4:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached at (571) 272-3667.

Central TC telephone number is (571) 272-2100.

The fax number for the organization is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Thuan N. Du
November 7, 2008

/Thuan N. Du/
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